TQMa6ULx
User's Manual

TQMa6ULx UM 0105
23.07.2020

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TABLE DIRECTORY

FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	16.01.2018	Petz		Initial release
0101	10.02.2018	Petz	All Table 2, Table 3 3.2.1.4, Table 5, Table 6, Table 7, Table 9, Table 10 2, 3, Table 14, Table 39, Figure 9 Figure 13 3.2.7.8 Table 43 Figure 20, Figure 21, Table 48	Typo and formatting Signal names corrected Information clarified Updated Colour of Reset LED added Warning added Added Updated
0102	04.04.2018	Petz	All Table 3 3.2.5.8, Table 28 3.2.5.14, 3.2.5.15	"QSPIA" replaced with "QSPI_A" Footnotes 11, and 12 added Completely reworked Content clarified
0103	18.06.2018	Petz	All 3.2.2.5 Figure 21	Hyperlinks updated Information regarding "D2" added Pin numbers added
0104	14.08.2019	Petz	All Table 2, SNVS_TAMPER GPIO1_IO18, GPIO1_IO19 QSPI 1.9 Footnote 12 Table 8 Table 17 3.2.5.7 Table 2, Table 34 Table 39 Figure 20, Table 43 Table 44, Table 45 3.2.2.4, 3.2.2.5	Hyperlinks updated, ® and ™ symbols added Function of i.MX6UL balls J14 and K15 corrected "Manufacturer" removed SNVS voltage changed from 3.3 V to 3.0 V Direction corrected Voltage level corrected IMX6ULCEC Data Sheet added Added High-Speed (HS) support added Moved from 3.2.2.5 to 3.2.2.4 Warning updated Direction of "USDHC1_WP" corrected Remarks clarified Updated "Package temperature" replaced with "Case temperature" Case temperature DDR3L SDRAM changed to +95 °C Renamed
0105	23.07.2020	Petz	1.9, 2, 2.1, Table 4 2, 2.1, Figure 1 Figure 2 1.9, 8.2 3.1.2 Table 16, Table 17 4.6	Information about i.MX6ULL CPUs added Updated Added Link to Yocto documentation added, links updated Chapters 3.12 and 3.1.3 merged Removed Statements rephrased

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa6ULx and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa6ULx schematics
- MBa6ULx User's Manual
- i.MX6UL and i.MX6ULL Data Sheets
- i.MX6UL and i.MX6ULL Reference Manuals
- IMX6ULCEC Data Sheet
- IMX6ULRM Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa6ULx

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa6ULx revision **02xx** and **03xx** in combination with the MBa6ULx revision 02xx and refers to some software settings. A certain TQMa6ULx version does not necessarily provide all features described in this User's Manual. This User's Manual does also not replace the NXP i.MX6UL documentation (Table 47).

The TQMa6ULx is a universal Minimodule based on the NXP Cortex®-A7 ARM CPU MCIMX6GxCVM05 i.MX6UL or i.MX6ULL.

The Cortex®-A7 core of this i.MX6UL is typically clocked with 528 MHz [1]

For reasons of clarity, it is not referred to the i.MX6ULL with every mention of the i.MX6UL in this User's Manual. If necessary, however, this will be pointed out.

2.1 Block diagram i.MX6UL, i.MX6ULL

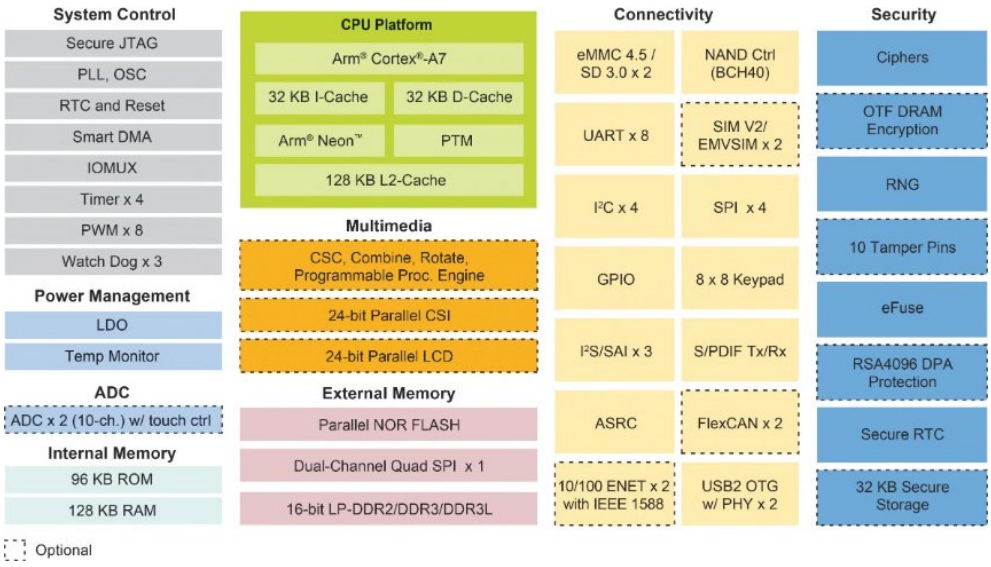


Figure 1: Block diagram i.MX6UL
(Source: NXP)

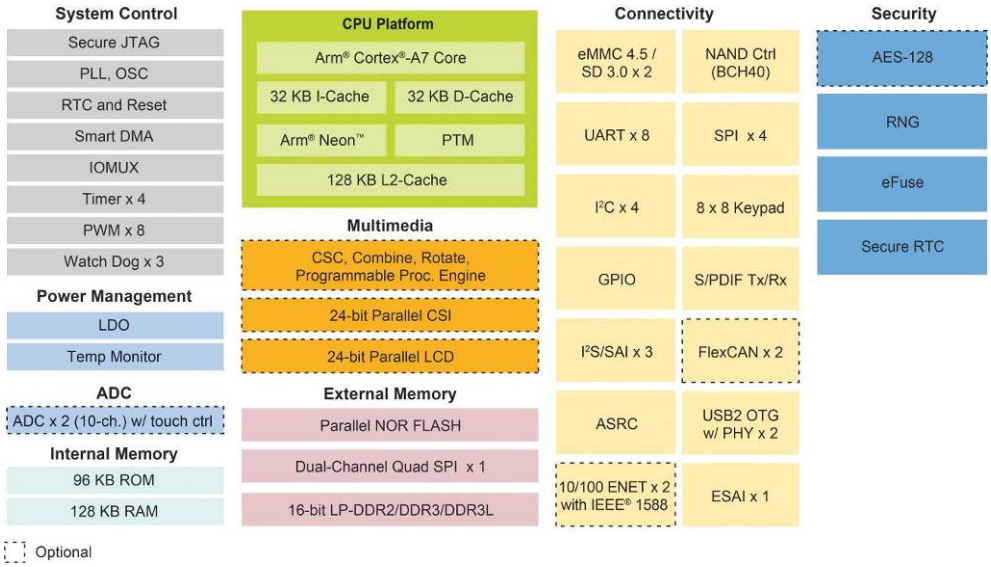


Figure 2: Block diagram i.MX6UL
(Source: NXP)

1: Up to 700 MHz with selected i.MX6UL.

2.1 Block diagram i.MX6UL, i.MX6ULL (continued)

The TQMa6ULx extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

A suitable i.MX6UL derivative (UL1, UL2 or UL3) can be selected for each requirement.

All essential i.MX6UL signals are routed to the connectors. There are therefore no restrictions for customers using the TQMa6ULx with respect to an integrated customised design. All essential components like i.MX6UL, DDR3L SDRAM, eMMC, and power management are already integrated on the TQMa6ULx.

The main features of the TQMa6ULx are:

- NXP i.MX6UL CPU
- Up to 1 Gbyte DDR3L SDRAM, with 16 bit data bus interface
- Up to 32 Gbyte eMMC NAND flash
- Up to 256 Mbyte QSPI NOR flash
- 64 kbit EEPROM
- EEPROM + temperature sensor
- NXP Power Management Integrated Circuit PF3000/ PF3001
- All essential i.MX6UL signals are routed to the TQMa6ULx connectors
- Extended temperature range
- Single supply voltage 5 V

The MBa6ULx serves as an evaluation board for the TQMa6ULx.

2.2 Key functions and characteristics

The following components are implemented on the TQMa6ULx:

- i.MX6UL CPU
- DDR3L 800 SDRAM
- eMMC NAND flash
- QSPI NOR flash
- EEPROM
- Temperature sensor + EEPROM
- RTC
- Supervisor with Reset structure
- Power supply by PMIC with Power Sequencing
- Two connectors (2 × 100 pins)

The following primary interfaces are provided at the TQMa6ULx connectors: [2]

- 2 × Ethernet 10/100 RMII
- 2 × I²C (1 × for the devices on the TQMa6ULx)
- 1 × JTAG
- 1 × Parallel LCD RGB 24-bit interface
- 2 × CAN
- 1 × SPI
- 2 × USB 2.0 OTG
- 11 × GPIO
- 3 × UART
- 1 × SD 4-bit (SDIO / MMC / SD card)
- 10 × Tamper
- 1 × differential clock (CCM)
- 1 × QSPI (for second SPI NOR flash; SS1)
- 1 × WDOG

By adapting the pin configuration, further i.MX6UL interfaces are also available as an alternative to the mentioned factory configuration. These are amongst other:

- Camera Sensor-Interfaces 8-bit (CSI – CMOS Sensor Interface)
- Synchronous Audio Interface (SAI – e.g., I²S)
- PWM
- ADC
- EIM bus (External Interface Module)
- Enhanced Periodic Interrupt Timer
- General Purpose Media Interface
- General Purpose Timer
- Key Pad Port
- More audio interfaces
- One more I²C interface
- More SPI interfaces
- More UARTs

2: Number of interfaces depend on i.MX6UL derivative.

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa6ULx, and the BSP provided by TQ-Systems. See also chapter 5.

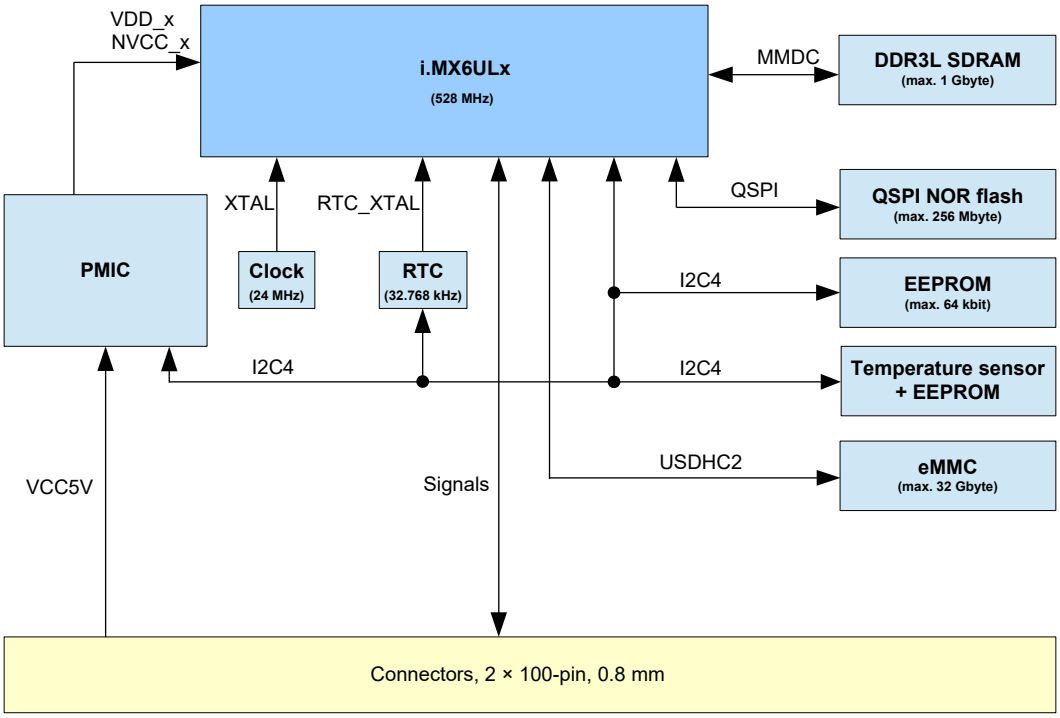


Figure 3: Block diagram TQMa6ULx (simplified)

3.1 Interfaces to other systems and devices

3.1.1 Pin multiplexing

The multiple pin configurations by different i.MX6UL-internal function units must be taken note of.
The pinout in Table 2 and Table 3 refers to the BSP provided by TQ-Systems in combination with the carrier board MBa6ULx.
NXP provides a tool showing the multiplexing and simplifies the selection and configuration (i.MX pins Tool – NXP Tool).
The electrical and pin characteristics are to be taken from the i.MX6UL Data Sheets (1), (2), (6), the Reference Manual (7), and the PMIC Data Sheet (10).

Attention: Malfunction or destruction, i.MX6UL pin multiplexing	
	Depending on the configuration, many i.MX6UL balls can provide several different functions. Please take note of the information concerning the configuration of these pins in the i.MX6UL Reference Manual (7), and the i.MX6UL Errata (2) before integration or start-up of your carrier board. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa6ULx.

3.1.2 Pinout TQMa6ULx connectors

Table 2: Pinout connector X1

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
–	P	5 V	Power	VCC5V	1	2	VCC5V	Power	5 V	P	–
–	P	5 V	Power	VCC5V	3	4	VCC5V	Power	5 V	P	–
–	P	5 V	Power	VCC5V	5	6	VCC5V	Power	5 V	P	–
–	P	0 V	Ground	DGND	7	8	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	9	10	LICELL [3]	Power	3.3 V	P	–
–	P	1.8 V	Power	VCC1V8_OUT	11	12	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	13	14	VCC3V3_V33_OUT	Power	3.3 V	P	–
–	P	3.0 V	Power	VSNVS_REF_OUT	15	16	DGND	Ground	0 V	P	–
–	P	3.3 V	Power	VCC3V3_REF_OUT	17	18	VCC2V5_OUT	Power	2.5 V	P	–
–	P	0 V	Ground	DGND	19	20	DGND	Ground	0 V	P	–
–	P	0.675 V	Power	VCCDDR_OUT	21	22	VCCCORE_OUT	Power	1.4 V	P	–
–	P	0 V	Ground	DGND	23	24	DGND	Ground	0 V	P	–
F4	P	1.8 or 3.3 V [4]	Power	NVCC_CSI	25	26	NVCC_ENET	Power	2.5 or 3.3 V [5]	P	F13
–	P	0 V	Ground	DGND	27	28	DGND	Ground	0 V	P	–
P17	O	2.5 V	CCM	CCM_CLK1_P	29	30	DGND	Ground	0 V	P	–
P16	O	2.5 V	CCM	CCM_CLK1_N	31	32	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	33	34	DGND	Ground	0 V	P	–
R8	I	3.3 V	Config	MX6UL_ONOFF	35	36	USB_OTG2_OC	USB	3.3 V	I	L17
T9	I	3.3 V	Config	PMIC_PWRON	37	38	USB_OTG2_PWR	USB	3.3 V	O	L14
–	P	0 V	Ground	DGND	39	40	DGND	Ground	0 V	P	–
U16	O	Open-Drain	USB	USB_OTG1_CHD#	41	42	USB_OTG2_VBUS	Power	5 V	P	U12
–	P	0 V	Ground	DGND	43	44	USB_OTG2_ID	USB	3.3 V	I	M17
T12	P	5 V	Power	USB_OTG1_VBUS	45	46	DGND	Ground	0 V	P	–
K13	I	3.3 V	USB	USB_OTG1_ID	47	48	USB_OTG2_DN	USB	3 V	I/O	T13
L15	I	3.3 V	USB	USB_OTG1_OC	49	50	USB_OTG2_DP	USB	3 V	I/O	U13
M16	O	3.3 V	USB	USB_OTG1_PWR	51	52	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	53	54	UART3_RX_DATA	UART	3.3 V	I	H16
T15	I/O	3 V	USB	USB_OTG1_DN	55	56	UART3_TX_DATA	UART	3.3 V	O	H17
U15	I/O	3 V	USB	USB_OTG1_DP	57	58	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	59	60	BOOT_MODE0	Boot	3.0 V [6]	I	T10
N8	I	3.0 V	SNVS	SNVS_TAMPER5	61	62	BOOT_MODE1	Boot	3.0 V [6]	I	U10
N11	I	3.0 V	SNVS	SNVS_TAMPER6	63	64	DGND	Ground	0 V	P	–
N10	I	3.0 V	SNVS	SNVS_TAMPER7	65	66	SNVS_TAMPER0	SNVS	3.0 V	I	R10
N9	I	3.0 V	SNVS	SNVS_TAMPER8	67	68	SNVS_TAMPER1	SNVS	3.0 V	I	R9
R6	I	3.0 V	SNVS	SNVS_TAMPER9	69	70	SNVS_TAMPER2	SNVS	3.0 V	I	P11
–	P	0 V	Ground	DGND	71	72	SNVS_TAMPER3	SNVS	3.0 V	I	P10
M14	I	3.3 V	JTAG	JTAG_TCK	73	74	SNVS_TAMPER4	SNVS	3.0 V	I	P9
P14	I	3.3 V	JTAG	JTAG_TMS	75	76	DGND	Ground	0 V	P	–
N16	I	3.3 V	JTAG	JTAG_TDI	77	78	JTAG_TDO	JTAG	3.3 V	O	N15
–	P	0 V	Ground	DGND	79	80	JTAG_TRST#	JTAG	3.3 V	I	N14
M15	I/O	3.3 V	GPIO	GPIO1_IO09	81	82	JTAG_MOD	JTAG	3.3 V	I	P15
K15	I/O	3.3 V	GPIO	GPIO1_IO18	83	84	DGND	Ground	0 V	P	–
J14	I/O	3.3 V	GPIO	GPIO1_IO19	85	86	UART1_RX_DATA	UART	3.3 V	I	K16
J16		3.3 V	I²C	I2C4_SDA	87	88	UART1_TX_DATA	UART	3.3 V	O	K14
J17		3.3 V	I²C	I2C4_SCL	89	90	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	91	92	CAN2_RX	CAN	3.3 V	I	H14
N17	O	3.3 V	Config	WDOG1#	93	94	CAN2_TX	CAN	3.3 V	O	J15
P8	I	3.3 V	Config	RESET_IN#	95	96	CAN1_RX	CAN	3.3 V	I	G14
–	O	3.3 V	Config	RESET_OUT#	97	98	CAN1_TX	CAN	3.3 V	O	H15
–	P	0 V	Ground	DGND	99	100	DGND	Ground	0 V	P	–

3: LICELL can be left open, if RTC backup or other functions of the SNVS domain are not required (see NXP documentation).
4: 1.8 V, if NVCC_CSI is connected to VCC1V8_OUT. 3.3 V, if NVCC_CSI is connected to VCC3V3_V33_OUT.
5: 2.5 V, if NVCC_ENET is connected to VCC2V5_OUT. 3.3 V, if NVCC_ENET is connected to VCC3V3_REF_OUT.
6: Use VSNVS_REF_OUT as reference voltage for BOOT-CFG resistors.

3.1.2 Pinout TQMa6ULx connector (continued)

Table 3: Pinout connector X2

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
–	P	0 V	Ground	DGND	1	2	DGND	Ground	0 V	P	–
G16	O	3.3 V	SPI	SPI2_SS0#	3	4	SPI2_MISO	SPI	3.3 V	I	G13
G17	O	3.3 V	SPI	SPI2_SCLK	5	6	SPI2_MOSI	SPI	3.3 V	O	F17
F15	O	2.5 / 3.3 V [7]	ENET	ENET1_TX_EN	7	8	DGND	Ground	0 V	P	–
F14	O	2.5 / 3.3 V [7]	ENET	ENET1_TX_CLK	9	10	ENET_MGMT_MDC	ENET	2.5 / 3.3 V [7]	O	L16
–	P	0 V	Ground	DGND	11	12	ENET_MGMT_MDIO	ENET	2.5 / 3.3 V [7]	I/O	K17
E15	O	2.5 / 3.3 V [7]	ENET	ENET1_TDATA0	13	14	ENET2_TX_CLK	ENET	2.5 / 3.3 V [7]	O	D17
E14	O	2.5 / 3.3 V [7]	ENET	ENET1_TDATA1	15	16	DGND	Ground	0 V	P	–
F16	I	2.5 / 3.3 V [7]	ENET	ENET1_RDATA0	17	18	ENET2_RX_ER	ENET	2.5 / 3.3 V [7]	I	D16
E17	I	2.5 / 3.3 V [7]	ENET	ENET1_RDATA1	19	20	ENET2_RDATA1	ENET	2.5 / 3.3 V [7]	I	C16
E16	I	2.5 / 3.3 V [7]	ENET	ENET1_RX_EN	21	22	ENET2_RDATA0	ENET	2.5 / 3.3 V [7]	I	C17
D15	I	2.5 / 3.3 V [7]	ENET	ENET1_RX_ER	23	24	ENET2_RX_EN	ENET	2.5 / 3.3 V [7]	I	B17
–	P	0 V	Ground	DGND	25	26	ENET2_TX_EN	ENET	2.5 / 3.3 V [7]	O	B15
B16	I/O	3.3 V [8]	LCD	LCD.DAT23	27	28	ENET2_TDATA0	ENET	2.5 / 3.3 V [7]	O	A15
A14	I/O	3.3 V [8]	LCD	LCD.DAT22	29	30	ENET2_TDATA1	ENET	2.5 / 3.3 V [7]	O	A16
B14	I/O	3.3 V [8]	LCD	LCD.DAT21	31	32	DGND	Ground	0 V	P	–
C14	I/O	3.3 V [8]	LCD	LCD.DAT20	33	34	LCD.DAT15	LCD	3.3 V [8]	I/O	D13
–	P	0 V	Ground	DGND	35	36	LCD.DAT14	LCD	3.3 V [8]	I/O	A12
D14	I/O	3.3 V [8]	LCD	LCD.DAT19	37	38	LCD.DAT13	LCD	3.3 V [8]	I/O	B12
A13	I/O	3.3 V [8]	LCD	LCD.DAT18	39	40	LCD.DAT12	LCD	3.3 V [8]	I/O	C12
B13	I/O	3.3 V [8]	LCD	LCD.DAT17	41	42	DGND	Ground	0 V	P	–
C13	I/O	3.3 V [8]	LCD	LCD.DAT16	43	44	LCD.DAT11	LCD	3.3 V [8]	I/O	D12
–	P	0 V	Ground	DGND	45	46	LCD.DAT10	LCD	3.3 V [8]	I/O	E12
D11	I/O	3.3 V [8]	LCD	LCD.DAT07	47	48	LCD.DAT09	LCD	3.3 V [8]	I/O	A11
A10	I/O	3.3 V [8]	LCD	LCD.DAT06	49	50	LCD.DAT08	LCD	3.3 V [8]	I/O	B11
B10	I/O	3.3 V [8]	LCD	LCD.DAT05	51	52	DGND	Ground	0 V	P	–
C10	I/O	3.3 V [8]	LCD	LCD.DAT04	53	54	LCD_CLK	LCD	3.3 V [8]	O	A8
–	P	0 V	Ground	DGND	55	56	DGND	Ground	0 V	P	–
D10	I/O	3.3 V [8]	LCD	LCD.DAT03	57	58	LCD_ENABLE	LCD	3.3 V [8]	O	B8
E10	I/O	3.3 V [8]	LCD	LCD.DAT02	59	60	LCD_RESET	LCD	3.3 V [8]	O	E9
A9	I/O	3.3 V [8]	LCD	LCD.DAT01	61	62	LCD_HSYNC	LCD	3.3 V [8]	O	D9
B9	I/O	3.3 V [8]	LCD	LCD.DAT00	63	64	LCD_VSYNC	LCD	3.3 V [8]	I/O	C9
–	P	0 V	Ground	DGND	65	66	QSPI_A_DATA0	QSPI	1.8 V	I/O	A3
B3	I/O	3.3 V	SD	SD1_DATA0	67	68	QSPI_A_DATA1	QSPI	1.8 V	I/O	C5
B2	I/O	3.3 V	SD	SD1_DATA1	69	70	QSPI_A_DATA2	QSPI	1.8 V	I/O	B5
B1	I/O	3.3 V	SD	SD1_DATA2	71	72	QSPI_A_DATA3	QSPI	1.8 V	I/O	A4
A2	I/O	3.3 V	SD	SD1_DATA3	73	74	QSPI_A_SS1# [9]	QSPI	1.8 V	O	A5
C2	I/O	3.3 V	SD	SD1_CMD	75	76	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	77	78	QSPI_A_SCK	QSPI	1.8 V	O	D5
C1	O	3.3 V	SD	SD1_CLK	79	80	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	81	82	QSPI_A_SS0# [10]	QSPI	1.8 V	O	E6
E4	I/O	1.8 / 3.3 V [11]	GPIO	GPIO4_IO21	83	84	DGND	Ground	0 V	P	–
E3	I/O	1.8 / 3.3 V [11]	GPIO	GPIO4_IO22	85	86	GPIO4_IO25	GPIO	1.8 / 3.3 V [11]	I/O	D4
–	P	0 V	Ground	DGND	87	88	GPIO4_IO26	GPIO	1.8 / 3.3 V [11]	I/O	D3
E2	I/O	1.8 / 3.3 V [11]	GPIO	GPIO4_IO23	89	90	GPIO4_IO27	GPIO	1.8 / 3.3 V [11]	I/O	D2
E1	I/O	1.8 / 3.3 V [11]	GPIO	GPIO4_IO24 [12]	91	92	GPIO4_IO28	GPIO	1.8 / 3.3 V [11]	I/O	D1
–	I	–	RFU	RFU1	93	94	DGND	Ground	0 V	P	–
F3	O	3.3 V	I²C	I2C2_SCL	95	96	UART6_RX_DATA	UART	3.3 V	I	E5
F2	I/O	3.3 V	I²C	I2C2_SDA	97	98	UART6_TX_DATA	UART	3.3 V	O	F5
–	P	0 V	Ground	DGND	99	100	DGND	Ground	0 V	P	–

7: 2.5 V, if NVCC_ENET is connected to VCC2V5_OUT. 3.3 V, if NVCC_ENET is connected to VCC3V3_REF_OUT.
8: Use VCC3V3_REF_OUT as reference voltage for BOOT-CFG resistors.
9: Only available on request, and when no **eMMC** is assembled on the TQMa6ULx.
10: Only available on request, and when no **QSPI NOR flash** is assembled on the TQMa6ULx.
11: 1.8 V, if NVCC_CSI is connected to VCC1V8_OUT. 3.3 V, if NVCC_CSI is connected to VCC3V3_V33_OUT.
12 : Signal can be connected to PMIC_INT# or TEMP_EVENT# as an assembly option. Default: None.

3.2 System components

3.2.1 i.MX6UL CPU

3.2.1.1 i.MX6UL derivatives

Depending on the TQMa6ULx version, one of the following i.MX6UL derivatives is assembled.

Table 4: i.MX6UL derivatives

CPU	Description	CPU clock	Temperature range
i.MX6UL	MCIMX6G1CVM	528 MHz	–40 °C … +105 °C
	MCIMX6G2CVM	528 MHz	–40 °C … +105 °C
	MCIMX6G3CVM	528 MHz	–40 °C … +105 °C
i.MX6ULL	MCIMX6Y0CVM	528 MHz	–40 °C … +105 °C
	MCIMX6Y1CVM	528 MHz	–40 °C … +105 °C
	MCIMX6Y2CVM	528 MHz	–40 °C … +105 °C

3.2.1.2 eFuses

The eFuses in the i.MX6UL are available for the user, except for the MAC address eFuses.

TQMa6ULx modules are delivered pre-programmed with MAC addresses from the TQ-Systems MAC address pool.

As of TQMa6ULx revision 0300, the MAC address LOCK-FUSE WP (Write Protect) is burnt, which permits to temporarily overwrite the MAC address for test purposes. If this is not desired, the MAC address LOCK-FUSE OP (Overwrite Protect) can be burned by the user.

3.2.1.3 i.MX6UL errata

Attention: Malfunction or destruction, i.MX6UL errata	
	Please take note of the current i.MX6UL errata (2).

3.2.1.4 Boot Modes

The i.MX6UL contains a ROM with integrated boot loader.
After power-up, the boot code initializes the hardware and then loads the program image from the selected boot device.
The eMMC or the QSPI NOR flash integrated on the TQMa6ULx can for example be selected as the standard boot device.
Additional boot interfaces are available as an alternative to booting from the integrated eMMC or the QSPI NOR flash, see 3.2.1.6.
More information about boot interfaces and its configuration is to be taken from the i.MX6UL Data Sheet (1) and the Reference Manual (7).
The boot device and its configuration, as well as different i.MX6UL settings have to be set via different boot registers.
Therefore, the i.MX6UL provides two possibilities:

- Burning internal eFuses
- Reading dedicated BOOT_CFG pins

The exact behaviour during booting depends on the value of register `BT_FUSE_SEL` (default = 0).
The following table shows the behaviour of `BT_FUSE_SEL` in dependence of the selected boot Mode.

Table 5: Boot Modes and BT_FUSE_SEL

BOOT_MODE[1:0]	Boot type	BT_FUSE_SEL	Usage
`00` (default)	Boot from eFuses	`BT_FUSE_SEL` = 0: Boot using Serial Loader (default) `BT_FUSE_SEL` = 1: Boot configuration is taken from eFuses	Series production
`01`	Serial Downloader	(n/a)	Development / production
`10`	Internal Boot	`BT_FUSE_SEL` = 0: Boot configuration is taken from BOOT_CFG pins (default) `BT_FUSE_SEL` = 1: Boot configuration is taken from eFuses	Development
`11`	Reserved	(n/a)	(n/a)

3.2.1.5 Boot configuration

Some general settings are done with some eFuses independent from the boot device.

Table 6: General boot settings

i.MX6UL		TQMa6ULx		
eFuse	Option	Setting [13]	Signal	Pin
BOOT_CFG1[7:0]	**Boot configuration 1:** Specific to selected boot Mode	–	LCD.DAT[7:0]	–
BOOT_CFG2[7:3] BOOT_CFG2[1:0]	**Boot configuration 2:** Specific to selected boot Mode	–	LCD.DAT[15:11] LCD.DAT[9:8]	–
BOOT_CFG2[2]	**Boot frequencies (ARM / DDR):** 0 = 500 / 400 MHz 1 = 250 / 200 MHz	0	LCD.DAT10	X2-46
BOOT_CFG3[7:0]	**Reserved**	–	–	–
BOOT_CFG4[6:0]	**Boot configuration 4:** Specific to selected boot Mode	–	LCD.DAT[22:16]	–
BOOT_CFG4[7]	**Debug loop:** 0 = Loop disabled 1 = Loop enabled	0	LCD.DAT23	X2-27

Note: Boot configuration	
	No boot device is configured on the TQMa6ULx.02xx at delivery.

3.2.1.6 Boot interfaces

In the next chapters, the configuration of the following boot devices is described:

- eMMC
- QSPI NOR flash
- SD card

13: Voltage level or condition of eFuse.

3.2.1.7 Boot device eMMC

Table 7: Boot configuration eMMC at USDHC2

i.MX6UL		TQMa6ULx		
eFuse	Option	Setting [14]	Signal	Pin
BOOT_CFG1[7]	**Boot Device Selection:** 01 = Boot from USDHC Interface	0	LCD.DAT07	X2-47
BOOT_CFG1[6]		1	LCD.DAT06	X2-49
BOOT_CFG1[5]	**SD/MMC Selection:** 0 = SD/eSD/SDXC 1 = MMC/eMMC	1	LCD.DAT05	X2-51
BOOT_CFG1[4]	**Fast Boot:** 0 = Regular 1 = Fast boot	0	LCD.DAT04	X2-53
BOOT_CFG1[3]	**MMC Speed:** 0x = Normal Speed Mode 1x = High Speed Mode	0	LCD.DAT03	X2-57
BOOT_CFG1[2]		0	LCD.DAT02	X2-59
BOOT_CFG1[1]	**eMMC Reset Enable:** 0 = No action 1 = eMMC reset enabled (SD_RST pin)	0	LCD.DAT01	X2-61
BOOT_CFG1[0]	**SD Loopback Clock Source Selection:** 0 = through SD pin 1 = direct	0	LCD.DAT00	X2-63
BOOT_CFG2[7]	**eMMC Bus Width:** 000 = 1-bit 001 = 4-bit 010 = 8-bit 101 = 4-bit DDR (MMC 4.4) 110 = 8-bit DDR (MMC 4.4)	0	LCD.DAT15	X2-34
BOOT_CFG2[6]		1	LCD.DAT14	X2-36
BOOT_CFG2[5]		0	LCD.DAT13	X2-38
BOOT_CFG2[4]	**Port Select:** 00 = USDHC1 01 = USDHC2	0	LCD.DAT12	X2-40
BOOT_CFG2[3]		1	LCD.DAT11	X2-44
BOOT_CFG2[2]	**Boot Frequencies (ARM / DDR):** 0 = 500 / 400 MHz 1 = 250 / 200 MHz	0	LCD.DAT10	X2-46
BOOT_CFG2[1]	**USDHC2 Voltage Selection:** 0 = 3.3 V 1 = 1.8 V	0	LCD.DAT09	X2-48

In addition to the mode listed above the following eMMC modes are supported at port USDHC2.

Table 8: USDHC2 modes eMMC

eMMC mode	1 bit	4 bit	8 bit	8 bit DDR
Normal Speed	Yes	Yes	Yes	Yes
High Speed (HS)	Yes	Yes	Yes	(n/a)

14: Voltage level or condition of eFuse.

3.2.1.8 Boot device QSPI NOR flash

Table 9: Boot configuration QSPI NOR flash at QSPI1

i.MX6UL		TQMa6ULx		
eFuse	Option	Setting [15]	Signal	Pin
BOOT_CFG1[7]	**Boot Device Selection:** 0001 = Boot from QuadSPI	0	LCD.DAT07	X2-47
BOOT_CFG1[6]		0	LCD.DAT06	X2-49
BOOT_CFG1[5]		0	LCD.DAT05	X2-51
BOOT_CFG1[4]		1	LCD.DAT04	X2-53
BOOT_CFG1[3]	**QuadSPI Interface Selection:** 0 = QSPI1 1 = Reserved	0	LCD.DAT03	X2-57
BOOT_CFG1[2]	**DDRSMP:** 000 = Default	0	LCD.DAT02	X2-59
BOOT_CFG1[1]		0	LCD.DAT01	X2-61
BOOT_CFG1[0]		0	LCD.DAT00	X2-63

15: Voltage level or condition of eFuse.

3.2.1.9 Boot device SD card

Table 10: Boot configuration SD card at USDHC1

i.MX6UL		TQMa6ULx		
eFuse	Option	Setting [16]	Signal	Pin
BOOT_CFG1[7]	**Boot Device Selection:** 01 = Boot from USDHC Interface	0	LCD.DAT07	X2-47
BOOT_CFG1[6]		1	LCD.DAT06	X2-49
BOOT_CFG1[5]	**SD/MMC Selection:** 0 = SD/eSD/SDXC 1 = MMC/eMMC	0	LCD.DAT05	X2-51
BOOT_CFG1[4]	**Fast Boot:** 0 = Regular 1 = Fast boot	0	LCD.DAT04	X2-53
BOOT_CFG1[3]	**SD Speed:** 00 = Normal/SDR12 01 = High/SDR25 10 = SDR50 11 = SDR104	0	LCD.DAT03	X2-57
BOOT_CFG1[2]		1	LCD.DAT02	X2-59
BOOT_CFG1[1]	**SD Power Cycle Enable:** 0 = No power cycle 1 = Enable via USDHC_RST pin	0	LCD.DAT01	X2-61
BOOT_CFG1[0]	**SD Loopback Clock Source Sel:** 0 = through SD pin 1 = direct	0	LCD.DAT00	X2-63
BOOT_CFG2[7]	**SD Calibration Step:** 00 = 0 delay cells 01 = 1 delay cells 10 = 2 delay cells 11 = 3 delay cells	0	LCD.DAT15	X2-34
BOOT_CFG2[6]		0	LCD.DAT14	X2-36
BOOT_CFG2[5]	**Bus Width:** 0 = 1-bit 1 = 4-bit	1	LCD.DAT13	X2-38
BOOT_CFG2[4]	**Port Select:** 00 = USDHC1 01 = USDHC2	0	LCD.DAT12	X2-40
BOOT_CFG2[3]		0	LCD.DAT11	X2-44
BOOT_CFG2[2]	**Boot Frequencies (ARM / DDR):** 0 = 500 / 400 MHz 1 = 250 / 200 MHz	0	LCD.DAT10	X2-46
BOOT_CFG2[1]	**USDHC Voltage Selection:** 0 = 3.3 V 1 = 1.8 V	0	LCD.DAT09	X2-48

In addition to the mode listed above the following SD card modes are supported at port USDHC1.

Table 11: USDHC1 SD card modes

SD mode	Fast boot	1 bit	4 bit
Normal Speed	Yes	Yes	Yes
High Speed	Yes	Yes	Yes
SDR50	(n/a)	(n/a)	(n/a)
SDR104	(n/a)	(n/a)	(n/a)

16: Voltage level or condition of eFuse.

3.2.2 Memory

3.2.2.1 DDR3L SDRAM

One DDR3L SDRAM chip is assembled on the TQMa6ULx.
The chip is connected to the i.MX6UL with 16 bit address and 16 bit data interface.
The following block diagram shows how the DDR3L SDRAM is connected to the i.MX6UL.

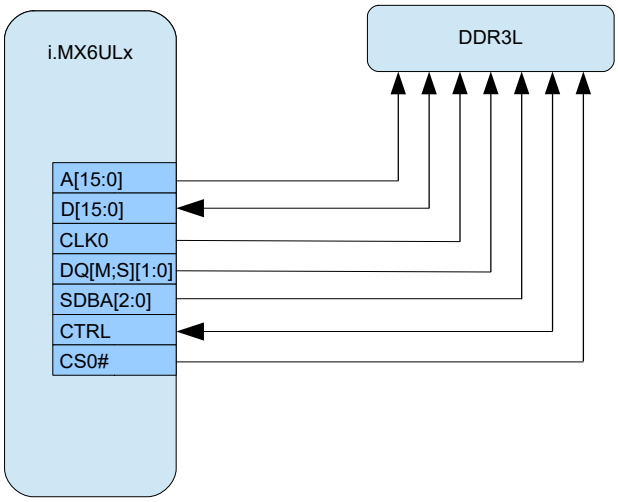


Figure 4: Block diagram DDR3L SDRAM interface

The memory interface characteristics are shown in the following table.

Table 12: i.MX6UL SDRAM interface

i.MX6UL derivative	Bus width	Frequency	No. of SDRAM chips
i.MX6UL	×16	400 MHz	1

The assembly options of DDR3L SDRAM on the TQMa6ULx are listed in the following table.

Table 13: DDR3L SDRAM

Manufacturer	Part number	Type	Temperature range
Micron	MT41K128M16JT-125 IT:K	DDR3L-1600 128M16	–40 °C … +95 °C
Samsung	K4B2G1646F-BMK0	DDR3L-1600 128M16	–40 °C … +95 °C

3.2.2.2 eMMC NAND flash

An eMMC NAND flash is provided for the boot loader and the application software.
The following block diagram shows how the eMMC flash is connected to the i.MX6UL and the connectors.

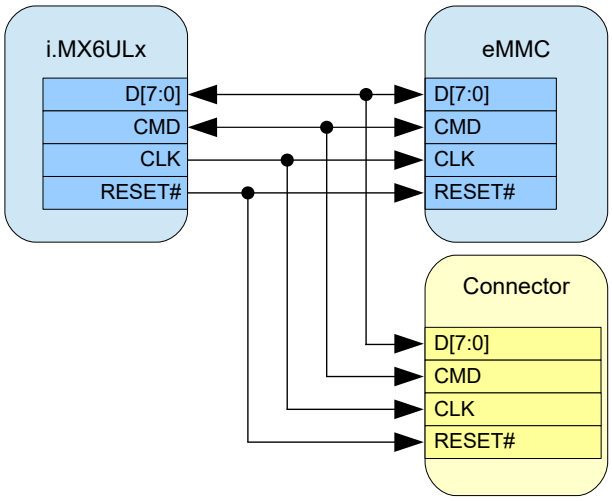


Figure 5: Block diagram eMMC interface

The support for the Hardware Reset-Function depends on the BSP.

The following table shows the eMMC devices, which can be assembled on the TQMa6ULx.

Table 14: eMMC NAND flash

Manufacturer	Part number	Type	Temperature range	Remark
Micron	MTFC4GACAJCN-1M	4 Gbyte / eMMC 5.0 / MLC	–25 °C … +85 °C	TQMa6ULx revision = 02xx
	MTFC4GACAJCN-4M		–40 °C … +85 °C	
	MTFC8GAKAJCN-1M WT	8 Gbyte / eMMC 5.0 / MLC	–25 °C … +85 °C	TQMa6ULx revision ≥ 03xx
	SDINBDG4-8G-T		–25 °C … +85 °C	

Attention: Malfunction or destruction, eMMC	
	The eMMC interface can only be used on the carrier board if the eMMC on the TQMa6ULx is not assembled.

3.2.2.3 QSPI NOR flash

A QSPI NOR flash is also available. It can e.g., serve as boot device or as recovery device.
The following block diagram shows how the QSPI NOR flash is connected to the i.MX6UL.

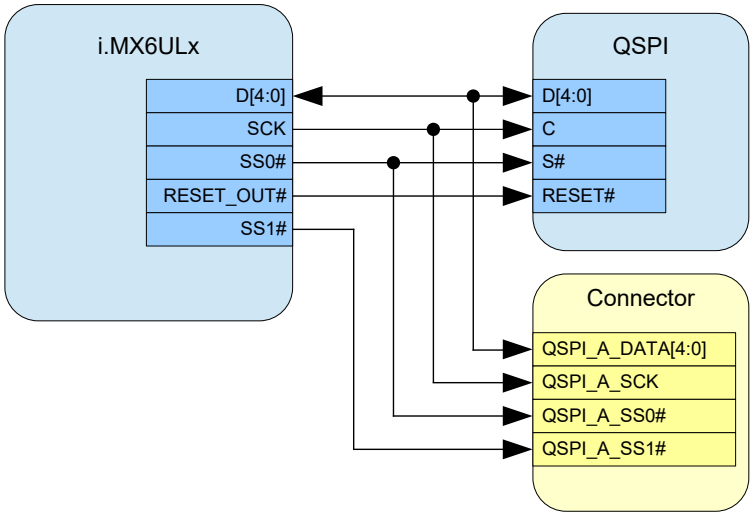


Figure 6: Block diagram QSPI NOR flash interface

The QSPI NOR flash Reset-Out pin as well as the QSPI signals are routed to the TQMa6ULx connectors.

The following table shows the QSPI NOR flash devices, which can be assembled on the TQMa6ULx.

Table 15: QSPI NOR flash

Manufacturer	Part number	Size		Temperature range
Micron	MT25QU512ABB8E12-0SIT	512 Mbit	64 Mbyte	–40 °C … +85 °C
Micron	MT25QU02GCBB8E12-0SIT	2048 Mbit	256 Mbyte	–40 °C … +85 °C

Attention: Malfunction or destruction, QSPI NOR flash	
	QSPI_A_SS1# is used as eMMC_DATA7 for the eMMC on the TQMa6ULx. The BSP provided by TQ-Systems supports the Extended I/O protocol in STR mode.

3.2.2.4 EEPROM 24LC64T

A serial EEPROM 24LC64T, controlled by the I2C4 bus, is assembled. Write-Protection (WP) is not supported by default but available as an assembly option. The following block diagram shows how the EEPROM 24LC64T is connected to the i.MX6UL.

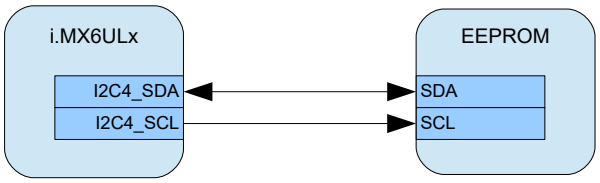


Figure 7: Block diagram EEPROM interface, 24LC64T

- The EEPROM has I²C address `0x50 / 101 0000b`

In the EEPROM, TQMa6ULx-specific data is stored. It is, however, not essential for the correct operation of the TQMa6ULx. The user can delete or alter the data. In the following table, the parameters stored in the EEPROM are shown.

Table 16: TQMa6ULx specific data in the EEPROM

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
0x00	Variable	Variable	$32_{(10)}$	Binary	Hard Reset Configuration Word (HRCW), (optional)
0x20	$6_{(10)}$	$10_{(10)}$	$16_{(10)}$	Binary	MAC address
0x30	$8_{(10)}$	$8_{(10)}$	$16_{(10)}$	ASCII	Serial number
0x40	Variable	Variable	$64_{(10)}$	ASCII	Order code
0x80	–	–	$8{,}064_{(10)}$	–	(Unused)

3.2.2.5 EEPROM with temperature sensor, SE97BTP

A serial EEPROM including temperature sensor, controlled by the I2C4 bus, is assembled on the TQMa6ULx.

The lower 128 bytes (addresses 00h to 7Fh) can be set to Permanent Write Protected (PWP) mode or Reversible Write-Protected (RWP) mode by software. The upper 128 bytes (addresses 80h to FFh) cannot be write-protected and can be used for general data storage. The EEPROM also provides a temperature sensor to monitor the temperature of the TQMa6ULx.

The SE97BTP (D2) is assembled on the top side of the TQMa6ULx, see Figure 21.

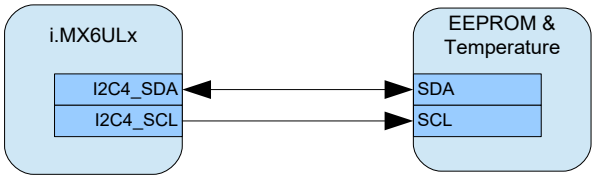


Figure 8: Block diagram EEPROM with temperature sensor, SE97BTP

- The device provides the following I²C addresses:
  - EEPROM (Normal Mode): `0x52 / 101 0010b`
  - EEPROM (Protected Mode): `0x32 / 011 0010b`
  - Temperature sensor: `0x1A / 001 1010b`

3.2.3 i.MX6UL-internal RTC

The i.MX6UL provides an RTC, which has its own power domain (SNVS).
The accuracy of the RTC is mainly determined by the characteristics of the quartz used.
The type FC-135 used on the TQMa6ULx has a standard frequency tolerance of ±20 ppm at +25 °C.
The following block diagram shows the implementation on the TQMa6ULx.

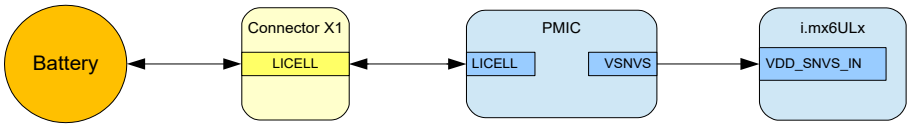


Figure 9: Block diagram i.MX6UL-internal RTC

The RTC power domain SNVS of the i.MX6UL is supplied by the PMIC-internal regulator VSNVS. This regulator is supplied either by VIN or by LICELL. LICELL supports simple coin cells as well as Lithium coin cells or SuperCaps, which can also be charged by the PMIC. Charging methods and electrical characteristics of the LICELL pin are to be taken from the PMIC Data Sheet (10).

Note: RTC power consumption	
	A coin cell is not suitable for long term bridging on account of the high current consumption. A Lithium coin cell or a SuperCap® might be an option depending on the use case. It is to be taken note of that the typical charging current is only 60 µA. For long term bridging the discrete RTC on the TQMa6ULx is recommended.

3.2.4 Discrete RTC

In addition to the i.MX6UL-internal RTC the TQMa6ULx provides a discrete RTC DS1339U, which is connected to I2C4.
The accuracy of the RTC is mainly determined by the characteristics of the quartz used.
The type CM7V-T1A used on the TQMa6ULx has a standard frequency tolerance of ±20 ppm at +25 °C.
The following block diagram shows the implementation on the TQMa6ULx.

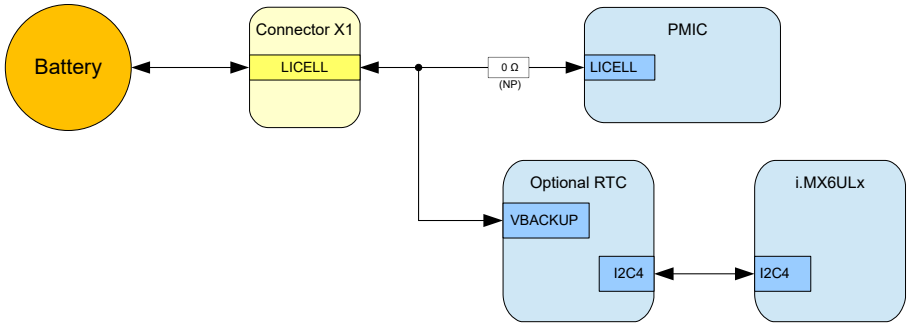


Figure 10: Block diagram discrete RTC

The discrete RTC is supplied with 3.3 V. VBACKUP of the RTC is available as LICELL at the connector.
LICELL supports simple coin cells as well as Lithium coin cells or SuperCaps, which can also be charged by the PMIC.
Charging methods and electrical characteristics of the LICELL pin are to be taken from the PMIC Data Sheet (10).

- The discrete RTC has I²C address `0x68 / 110 1000b`

Note: RTC power consumption	
	It is to be taken note of that the typical charging current is only 60 µA. A Lithium coin cell is recommended for long term bridging of the discrete RTC.

3.2.5 Interfaces

3.2.5.1 Overview

The TQMa6ULx provides interfaces with primary functions. They can all be used simultaneously independent of their configuration. Some primary functions are not available if a secondary function is used (e.g. EIM bus).
In the following chapters, only the external primary interfaces are described.

Table 17: Internal interfaces

Interface	Qty.	Function	Chapter	Remark
USDHC	1	Primary	3.2.5.13	USDHC2 | eMMC, 8 data bits
MMDC	1	Primary	3.2.2.1	DDR3L SDRAM, 16 data bits
QSPI	1	Primary	3.2.2.3	QSPI NOR flash, 4 data bits

Table 18: External interfaces

Interface	Qty.	Function	Chapter	Remark
CCM	2	Secondary	–	Multiplexing has to be adapted
CSI	1	Secondary	–	Multiplexing has to be adapted
ECSPI	1	Primary	3.2.5.2	ECSPI2
ECSPI	2	Secondary	3.2.5.2	ECPSI1 / ECSPI3 / ECSPI4 | Multiplexing has to be adapted
EIM	1	Secondary	–	Multiplexing has to be adapted
ENET	2	Primary	3.2.5.3	RMII (10/100 Mbit/s) / 1588 | Multiplexing has to be adapted
EPIT	2	Secondary	–	Multiplexing has to be adapted
FLEXCAN	2	Primary	3.2.5.4	FLEXCAN[2:1]
GPIO	11	Primary	3.2.5.5	GPIO1 / GPIO4
GPT	2	Secondary	–	GPT[2:1] | Multiplexing has to be adapted
I^2C	2	Primary	3.2.5.6	I2C2 / I2C4
I^2C	2	Secondary	3.2.5.6	I2C1 / I2C3 | Multiplexing has to be adapted
KPP	1	Secondary	–	Multiplexing has to be adapted
LCDIF	1	Primary	3.2.5.7	Graphics interface
MQS	1	Secondary	–	Multiplexing has to be adapted
NAND	1	Secondary	–	Multiplexing has to be adapted
PWM	8	Secondary	–	PWM[8:1] | Multiplexing has to be adapted
QSPI	4	Secondary	3.2.5.8	Multiplexing has to be adapted
SAI	3	Secondary	–	SAI[3:1] | Multiplexing has to be adapted
SIM	2	Secondary	–	Multiplexing has to be adapted
SJC	1	Primary	3.2.5.9	JTAG
SNVS	1	Primary	3.2.5.10	SNVS_TAMPER[9-0]
SPDIF	1	Secondary	–	Multiplexing has to be adapted
SRC	1	Secondary	–	Depends on BOOT_MODE0 | BOOT_MODE1
UART	3	Primary	3.2.5.11	UART1 / UART3 / UART6
UART	5	Secondary	3.2.5.11	UART2 / UART4 / UART[8:7] | Multiplexing has to be adapted
USB	2	Primary	3.2.5.12	USB_OTG1 / USB_OTG2
USDHC	1	Primary	3.2.5.13	SD card-Interface
WDOG	1	Primary	3.2.5.14	WDOG1#
WDOG	2	Secondary	3.2.5.14	WDOG[3:2]# | Multiplexing has to be adapted
XTALOSC	1	Primary	3.2.5.15	CCM_CLK1_N / CCM_CLK1_P

3.2.5.2 ECSPI

The i.MX6UL provides four full-duplex ECSPI interfaces, which can also be configured as Master/Slave.
Primarily ECSPI2 is available at the TQMa6ULx connectors.
The following table shows the signals used by the ECSPI2 interface.

Table 19: ECSPI2 signals

Signal name	Direction	i.MX6UL ball	TQMa6ULx
ECSPI2_MISO	I	G13	X2-4
ECSPI2_MOSI	O	F17	X2-6
ECSPI2_SCLK	O	G17	X2-5
ECSPI2_SS0#	O	G16	X2-3

3.2.5.3 ENET

The i.MX6UL provides a 10/100 MAC core, which supports MII (4 bit) and RMII (2 bit).
The RMII signals are available as primary function at the TQMa6ULx connectors.
The following table shows the signals used by the RMII interface.

Table 20: RMII signals

Signal name	Power-Group	Direction	i.MX6UL ball	TQMa6ULx
ENET_MDC	NVCC_GPIO (3.3 V)	O	L16	X2-10
ENET_MDIO		I/O	K17	X2-12
ENET1_RDATA0	NVCC_ENET (2.5 V or 3.3 V)	I	F16	X2-17
ENET1_RDATA1		I	E17	X2-19
ENET1_RX_EN		I	E16	X2-21
ENET1_RX_ER		I	D15	X2-23
ENET1_TDATA0		O	E15	X2-13
ENET1_TDATA1		O	E14	X2-15
ENET1_TX_CLK		O	F14	X2-9
ENET1_TX_EN		O	F15	X2-7
ENET2_RDATA0		I	C17	X2-22
ENET2_RDATA1		I	C16	X2-20
ENET2_RX_EN		I	B17	X2-24
ENET2_RX_ER		I	D16	X2-18
ENET2_TDATA0		O	A15	X2-28
ENET2_TDATA1		O	A16	X2-30
ENET2_TX_CLK		O	D17	X2-14
ENET2_TX_EN		O	B15	X2-26

Note: NVCC_ENET, VCC3V3_REF_OUT	
	NVCC_ENET has to be connected externally! VCC3V3_REF_OUT supplies an RMII PHY on the MBa6ULx with approximately 60 mA. It has to be ensured that the load on the customer's carrier board will also not be higher than approximately 60 mA.

The i.MX6UL RMII interface can operate with an I/O voltage of 2.5 V or 3.3 V. In order to use the interface, additional signals of the ENET signal group are required. The accompanying power supply pin is routed to pin X1-26 to operate these signals on the same I/O voltage, if RMII is used.

The MII interface can be used with an adapted pin multiplexing. Details are to be taken from the Reference Manual and the i.MX6UL Data Sheet (1), (7).

3.2.5.4 CAN

The i.MX6UL provides two integrated CAN 2.0B controllers. Both signals pairs are available at the TQMa6ULx connectors.
The drivers required have to be implemented on the carrier board.
The following table shows the signals used by the CAN interface.

Table 21: FLEXCAN signals

Signal name	Direction	i.MX6UL ball	TQMa6ULx
FLEXCAN1_RX	I	G14	X1-96
FLEXCAN1_TX	O	H15	X1-98
FLEXCAN2_RX	I	H14	X1-92
FLEXCAN2_TX	O	J15	X1-94

3.2.5.5 GPIO

Beside their interface function, most i.MX6UL pins can also be configured as GPIO.
All GPIOs can trigger an interrupt. The electrical characteristics of the GPIOs are to be taken from the i.MX6UL Reference Manual and Data Sheet (1), (7). Several pins are available as GPIO at the TQMa6ULx connectors.
The following table shows the GPIO signals provided.

Table 22: GPIO signals

Signal name	Power-Group	Direction	i.MX6UL ball	TQMa6ULx	Remark
GPIO1_IO09	3.3 V	I/O	M15	X1-81	–
GPIO1_IO18		I/O	K15	X1-83	Alternative function: USDHC1_WP
GPIO1_IO19		I/O	J14	X1-85	Alternative function: USDHC1_CD#
GPIO4_IO21	NVCC_CSI (1.8 V or 3.3 V)	I/O	E4	X2-83	–
GPIO4_IO22		I/O	E3	X2-85	–
GPIO4_IO23		I/O	E2	X2-89	–
GPIO4_IO24 [17]		I/O	E1	X2-91	Assembly option: PMIC_INT# or TEMP_EVENT#
GPIO4_IO25		I/O	D4	X2-86	–
GPIO4_IO26		I/O	D3	X2-88	–
GPIO4_IO27		I/O	D2	X2-90	–
GPIO4_IO28		I/O	D1	X2-92	–

Note: NVCC_CSI	
	NVCC_CSI has to be connected externally!

17: Can be used as temperature and PMIC interrupt. For more information please contact TQ-Support.

3.2.5.6 I²C

The i.MX6UL provides four I²C interfaces.
I2C2 and I2C4 are routed to the TQMa6ULx connectors and are available as primary function.
The following table shows the signals used by the I²C interfaces I2C2 and I2C4.

Table 23: I²C signals

Signal name	Direction	i.MX6UL ball	TQMa6ULx	Power-Group	Remark
I2C2_SCL	O	F3	X2-95	NVCC_CSI (1.8 V or 3.3 V)	–
I2C2_SDA	I/O	F2	X2-97		–
I2C4_SCL	O	J17	X1-89	3.3 V	2.2 kΩ PU to 3.3 V on TQMa6ULx
I2C4_SDA	I/O	J16	X1-87		2.2 kΩ PU to 3.3 V on TQMa6ULx

Note: NVCC_CSI	
	NVCC_CSI has to be connected externally!

The following table shows the I²C devices connected to the I2C4 bus on the TQMa6ULx.

Table 24: I²C addresses

Component	Function	Hex / 7-bit address	Remark
M24C64	EEPROM	0x50 / 101 0000b	–
PF3000	PMIC	0x08 / 000 1000b	Should not be altered
DS1339U	RTC (optional)	0x68 / 110 1000b	Assembly option
SE97BTP	EEPROM	0x52 / 101 0010b	Normal Mode
	EEPROM	0x32 / 011 0010b	Protection Mode
	Temperature sensor	0x1A / 001 1010b	–

If more devices are connected to the I²C buses on the carrier board, the maximum capacitive bus load according to the I²C standard has to be taken note of. If necessary, additional Pull-Ups at the I²C bus should be provided on the carrier board.

3.2.5.7 eLCDIF

The i.MX6UL provides a display controller, which supports displays of different size and performance.
Information regarding supported displays and formats are to be taken from the i.MX6UL Reference Manual (7).
The LCD signals are routed to the TQMa6ULx connectors as primary function.
The following table shows the signals used by the LCD interface.

Table 25: LCD signals

Signal name	Direction	i.MX6UL ball	TQMa6ULx
LCDIF_CLK	O	A8	X2-54
LCDIF_ENABLE	O	B8	X2-58
LCDIF_RESET	O	E9	X2-60
LCDIF_HSYNC	O	D9	X2-62
LCDIF_VSYNC	O	C9	X2-64
LCDIF_DATA23	I/O	B16	X2-27
LCDIF_DATA22	I/O	A14	X2-29
LCDIF_DATA21	I/O	B14	X2-31
LCDIF_DATA20	I/O	C14	X2-33
LCDIF_DATA19	I/O	D14	X2-37
LCDIF_DATA18	I/O	A13	X2-39
LCDIF_DATA17	I/O	B13	X2-41
LCDIF_DATA16	I/O	C13	X2-43
LCDIF_DATA15	I/O	D13	X2-34
LCDIF_DATA14	I/O	A12	X2-36
LCDIF_DATA13	I/O	B12	X2-38
LCDIF_DATA12	I/O	C12	X2-40
LCDIF_DATA11	I/O	D12	X2-44
LCDIF_DATA10	I/O	E12	X2-46
LCDIF_DATA09	I/O	A11	X2-48
LCDIF_DATA08	I/O	B11	X2-50
LCDIF_DATA07	I/O	D11	X2-47
LCDIF_DATA06	I/O	A10	X2-49
LCDIF_DATA05	I/O	B10	X2-51
LCDIF_DATA04	I/O	C10	X2-53
LCDIF_DATA03	I/O	D10	X2-57
LCDIF_DATA02	I/O	E10	X2-59
LCDIF_DATA01	I/O	A9	X2-61
LCDIF_DATA00	I/O	B9	X2-63

Attention: Malfunction or destruction, faulty boot process	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed. Suitable precautions have to be implemented on the carrier board to avoid violations caused e.g. by a display connected at the boot configuration pins. It also has to be ensured that the circuitry at the boot configuration pins (e.g., Pull-Downs) does not interfere with the function of a display connected at these pins.

3.2.5.8 QSPI

The optional QSPI NOR flash on the TQMa6ULx is connected to the i.MX6UL QSPI interface.
The QSPI interface is also routed to TQMa6ULx connector X2 to add more NOR flash on the carrier board.
QSPI_A_SS1# is only available on request and when no eMMC is assembled on the TQMa6ULx.
The following table shows the signals used by the QSPI interface.

Table 26: QSPI signals

Signal name	Direction	i.MX6UL ball	TQMa6ULx	Remark
QSPI_A_DATA3	I/O	A4	X2-72	–
QSPI_A_DATA2	I/O	B5	X2-70	–
QSPI_A_DATA1	I/O	C5	X2-68	–
QSPI_A_DATA0	I/O	A3	X2-66	–
QSPI_A_SS1#	O	A5	X2-74	Only available on request, and when **no eMMC** is assembled on the TQMa6ULx
QSPI_A_SS0#	O	E6	X2-82	Only available on request, and when **no QSPI NOR** is assembled on the TQMa6ULx
QSPI_A_SCK	O	D5	X2-78	–

Attention: Malfunction or destruction, QSPI interface	
	The QSPI signal pins of the TQMa6ULx have to be treated as NC, if not used on the carrier board. QSPI_A_SS1# can only be used on the carrier board, if no eMMC is assembled on the TQMa6ULx. The QSPI interface may only be used as a memory interface. SPI devices can be connected to the eCSPI interfaces.

3.2.5.9 SJC

The i.MX6UL provides two different JTAG modes. The pin JTAG_MOD defines the mode.
The following table shows the modes as well as the mode set on the TQMa6ULx.

Table 27: JTAG modes

JTAG_MOD	Name	Remark
0 (default)	Daisy Chain All	For common SW debug (High speed and series production)
1	SJC only	IEEE® 1149.1 JTAG compliant mode

The following table shows the signals used by the JTAG interface.

Table 28: JTAG signals

Signal name	Direction	i.MX6UL ball	TQMa6ULx	Remark
JTAG_TCK	I	M14	X1-73	i.MX6UL-internal 47 kΩ PU
JTAG_TMS	I	P14	X1-75	i.MX6UL-internal 47 kΩ PU
JTAG_TDI	I	N16	X1-77	i.MX6UL-internal 47 kΩ PU
JTAG_TDO	O	N15	X1-78	i.MX6UL-internal keeper
JTAG_TRST#	I	N14	X1-80	i.MX6UL-internal 47 kΩ PU
JTAG_MOD	I	P15	X1-82	4.7 kΩ PD on TQMa6ULx + i.MX6UL-internal 100 kΩ PU

3.2.5.10 TAMPER

The i.MX6UL provides protection against unauthorised opening or manipulation of a device by tamper detection.
The TAMPER pins are available for this purpose at the TQMa6ULx connectors.
Details about the TAMPER pins function are to be taken from the i.MX6UL Reference Manual (7).
The following table shows the available signals.

Table 29: TAMPER signals

Signal name	Direction	i.MX6UL ball	TQMa6ULx
SNVS_TAMPER9	I	R6	X1-69
SNVS_TAMPER8	I	N9	X1-67
SNVS_TAMPER7	I	N10	X1-65
SNVS_TAMPER6	I	N11	X1-63
SNVS_TAMPER5	I	N8	X1-61
SNVS_TAMPER4	I	P9	X1-74
SNVS_TAMPER3	I	P10	X1-72
SNVS_TAMPER2	I	P11	X1-70
SNVS_TAMPER1	I	R9	X1-68
SNVS_TAMPER0	I	R10	X1-66

3.2.5.11 UART

The i.MX6UL provides eight UART interfaces. Handshake signals are not available as primary function.
More UARTs as well as handshake signals can be configured in the multiplexing.
Details are to be taken from the i.MX6UL Reference Manual (7).

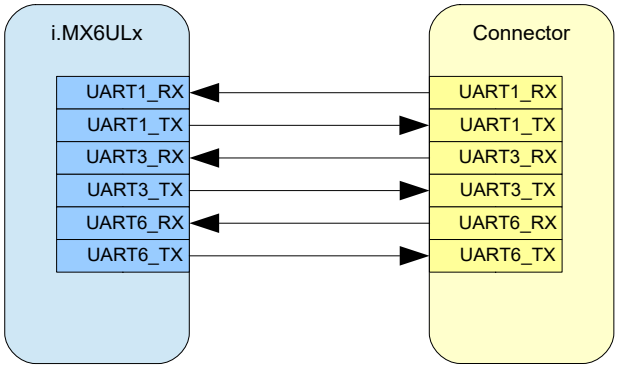


Figure 11: Block diagram UART interfaces

The following table shows the signals used by the UART interfaces.

Table 30: UART signals

Signal name	Direction	i.MX6UL ball	TQMa6ULx
UART1_RX_DATA	I	K16	X1-86
UART1_TX_DATA	O	K14	X1-88
UART3_RX_DATA	I	H16	X1-54
UART3_TX_DATA	O	H17	X1-56
UART6_RX_DATA	I	E5	X2-96
UART6_TX_DATA	O	F5	X2-98

Note: UART1	
	UART1 is configured as RS-232 on the MBa6ULx.

3.2.5.12 USB

The i.MX6UL provides two independent USB-OTG controllers with integrated High-Speed PHY.
Both USB-OTG controllers can operate in Host or in Device mode.
They are both available at the TQMa6ULx connectors as primary function.
The following table shows the signals used by the USB_OTG interfaces:

Table 31: USB_OTG signals

Signal name	Direction	i.MX6UL ball	TQMa6ULx	Remark
USB_OTG1_CHD#	I	U16	X1-41	–
USB_OTG1_ID	I	K13	X1-47	Device Mode: USB_OTG_ID signal is high Host Mode: USB_OTG_ID signal is low
USB_OTG1_OC	I	L15	X1-49	–
USB_OTG1_PWR	O	M16	X1-51	–
USB_OTG1_VBUS	P	T12	X1-45	–
USB_OTG1_DN	I/O	T15	X1-55	–
USB_OTG1_DP	I/O	U15	X1-57	–
USB_OTG2_ID	I	M17	X1-44	Device Mode: USB_OTG_ID signal is high Host Mode : USB_OTG_ID signal is low
USB_OTG2_OC	I	L17	X1-36	–
USB_OTG2_PWR	O	L14	X1-38	–
USB_OTG2_VBUS	P	U12	X1-42	–
USB_OTG2_DN	I/O	T13	X1-48	–
USB_OTG2_DP	I/O	U13	X1-50	–

Note: USB mode	
	Currently the BSP provided by TQ-Systems only supports Host mode.

3.2.5.13 USDHC

The i.MX6UL provides a USDHC controller, which is the interface between Host system and SD/SDIO/MMC cards.
The i.MX6UL USDHC1 port is routed to the TQMa6ULx connectors to connect an MMC, SD or SDIO card.

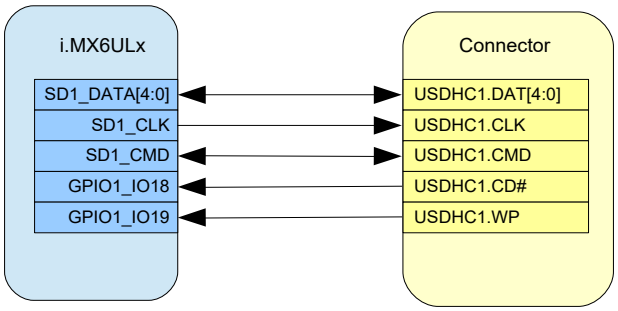


Figure 12: Block diagram USDHC interface

The following table shows the signals used by the USDHC interface.

Table 32: USDHC1 signals

Signal name	Direction	i.MX6UL ball	TQMa6ULx	Remark
USDHC1_CLK	O	C1	X2-79	–
USDHC1_CMD	I/O	C2	X2-75	–
USDHC1_DATA3	I/O	A2	X2-73	–
USDHC1_DATA2	I/O	B1	X2-71	–
USDHC1_DATA1	I/O	B2	X2-69	–
USDHC1_DATA0	I/O	B3	X2-67	–
USDHC1_CD#	I	J14	X1-85	Default: Muxed as GPIO1_IO18
USDHC1_WP	I	K15	X1-83	Default: Muxed as GPIO1_IO19

3.2.5.14 WDOG

The i.MX6UL provides three watchdog timers. Output WDOG1# is routed to TQMa6ULx connector X1-93.

The following table shows details of signal WDOG1#.

Table 33: Signal WDOG1#

Signal name	Direction	i.MX6UL ball	TQMa6ULx
WDOG1#	O	N17	X1-93

Only with signal WDOG1# software warm resets can be processed.
If a watchdog is required, TQMa6ULx signal WDOG1# must be routed to MR# of e.g., a TPS3808G33 on the carrier board.
The output of the TPS3808G33 must be routed to TQMa6ULx RESET_IN# in order to trigger a defined hard reset.

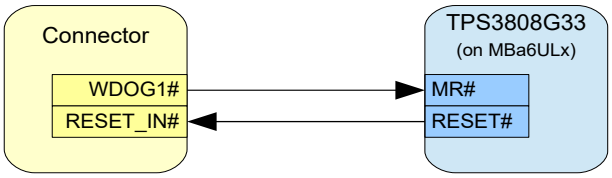


Figure 13: Block diagram WDOG1#

3.2.5.15 XTAL

The i.MX6UL provides a programmable differential clock output, which is routed to the TQMa6ULx connectors.
CCM_CLK1_N/P can be configured as differential (LVDS) clock input or clock output.

The following table shows details of the XTAL signals.

Table 34: XTAL signals

Signal name	Direction	i.MX6UL ball	TQMa6ULx
CCM_CLK1_N	O	P16	X1-31
CCM_CLK1_P	O	P17	X1-29

3.2.6 Reset signals

Reset inputs or outputs are available at the TQMa6ULx connectors. A red LED on the TQMa6ULx indicates the RESET# condition. The following block diagram shows the wiring of the reset signals.

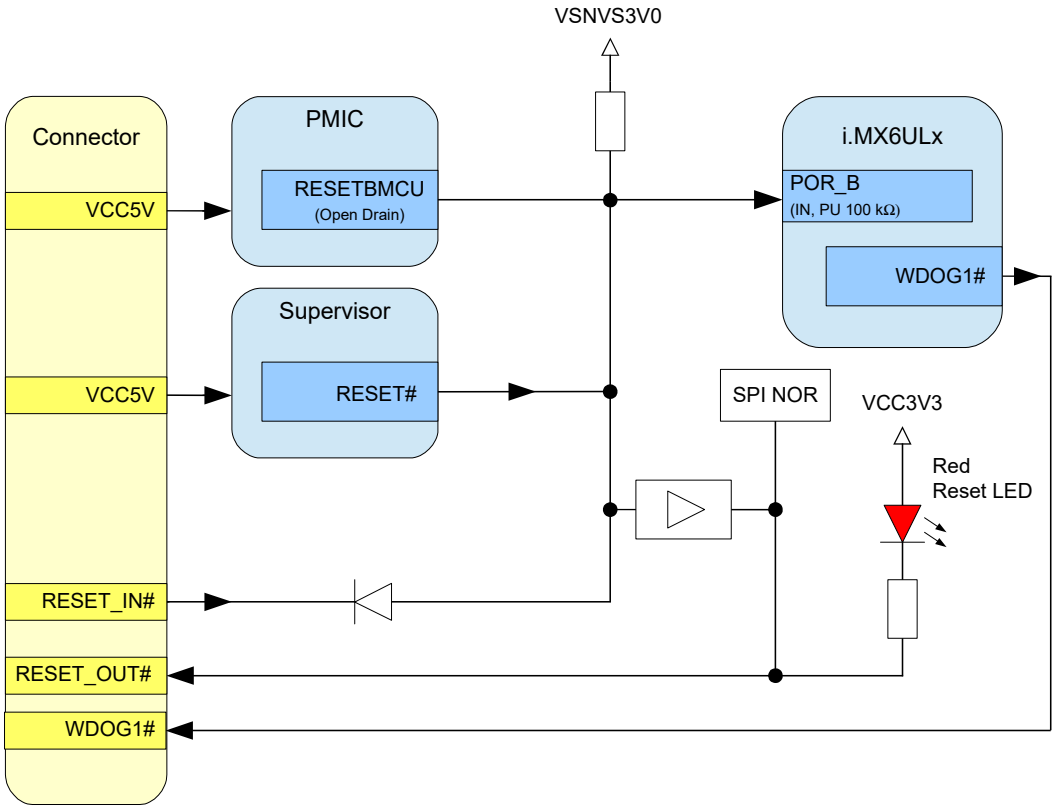


Figure 14: Block diagram Reset

The following table describes the reset signals available at the connectors:

Table 35: Reset signals

Signal name	Direction	i.MX6UL ball	TQMa6ULx	Remark
RESET_IN#	I_{PU_100k}	P8	X1-95	• Low-active signal • Reset input POR_B (Power-On Reset) of the i.MX6UL • COLD-resets the i.MX6UL • Minimal duration to trigger a reliable Reset: app. 30 µs, see (7)
RESET_OUT#	O	–	X1-97	• Reset output RESETBMCU of the PMIC • Can be used to reset external periphery
WDOG1#	O	N17	X1-93	• Low-active signal • Resets the i.MX6UL in case of an error

Other RESET# sources are:

- VIN – RESET#
- PMIC – RESETBMCU

3.2.7 Power supply

3.2.7.1 TQMa6ULx power supply

The following block diagram shows the TQMa6ULx power supply.
The TQMa6ULx requires a supply voltage of 5 V ±10 %.

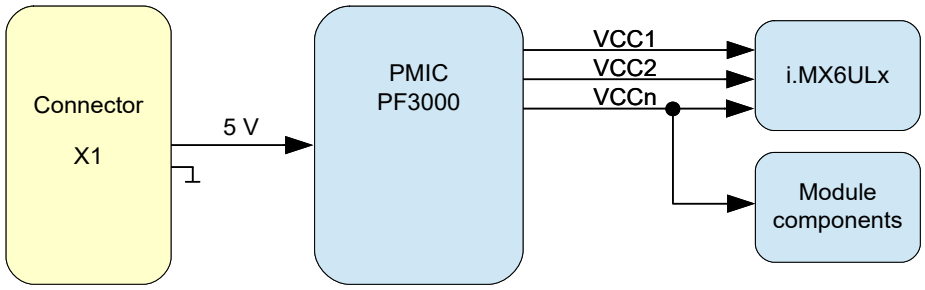


Figure 15: Block diagram TQMa6ULx power supply

The characteristics and functions of the single pins and signals are to be taken from the PMIC Data Sheet (10) and the i.MX6UL Reference Manual (7).

3.2.7.2 TQMa6ULx power consumption

The power consumption of the TQMa6ULx strongly depends on the application, the mode of operation and the operating system. For this reason the given values have to be seen as approximate values.
The following table shows power supply and power consumption parameters of the TQMa6ULx:

Table 36: TQMa6ULx power consumption

Mode of operation	Current at 5 V	Power at 5 V	Remark
Theoretical calculated peak	1330 mA	6650 mW	–
U-Boot prompt	103 mA	515 mW	–
Linux prompt	76 mA	380 mW	–
Linux stress test	143 mA	715 mW	No external interfaces active
Suspend to RAM	17 mA	85 mW	–
Standby	26 mA	130 mW	–

3.2.7.3 Voltage monitoring

The TQMa6ULx features a supervisor which monitors the input voltage (VCC5V). If the input voltage is too low, a Reset is triggered until the input voltage is in the permitted range again. The block diagram in Figure 14 shows the wiring.
The Supervisor triggers typically at 4.55 V (min: 4.45 V / max: 4.65 V) and adds a delay of 200 msec. All other voltages generated on the TQMa6ULx are routed to the TQMa6ULx connectors and can be monitored on the carrier board.

Attention: Malfunction or destruction, supply voltage exceedance	
	The voltage monitoring does not detect an exceedance of the permitted input voltage. An exceedance of the permitted input voltage may cause malfunction, destruction or accelerated ageing of the TQMa6ULx.

3.2.7.4 TQMa6ULx supply voltages

In addition to the TQMa6ULx supply voltage (VCC5V), some internal voltages are provided at the TQMa6ULx connectors.
The following table shows the voltages provided.

Table 37: TQMa6ULx supply voltages

Voltage	TQMa6ULx	Remark
LICELL	X1-10	RTC supply voltage. Connected to PMIC-RTC or discrete DS1339U RTC. See chapter 3.2.3, and 3.2.4
NVCC_CSI	X1-25	1.8 V or 3.3 V supply input
NVCC_ENET	X1-26	1.8 V or 3.3 V supply input
VCC1V8_OUT	X1-11	Max. load 100 mA
VCC2V5_OUT	X1-18	Max. load 100 mA
VCC3V3_REF_OUT	X1-17	Pull-Up voltage for LCD.DAT[24:0] „Enable“ for VCC3V3 (3.3 V) switch-through
VCC3V3_V33_OUT	X1-14	Reference only, do not apply additional load
VCCCORE_OUT	X1-22	Reference only, do not apply additional load
VCCDDR_OUT	X1-21	Reference only, do not apply additional load
VSNVS_REF_OUT	X1-15	Pull-Up voltage for BOOTMODE[1:0] Pull-Up voltage for EXT_WAKEUP

3.2.7.5 Other supply voltages

The TQMa6ULx also provides voltage inputs for the USB OTG controllers.

Table 38: TQMa6ULx USB_OTG supply voltages

Signal name	Direction	TQMa6ULx	Remark
USB_OTG1_VBUS	P	X1-45	VBUS voltage for USB controller For details see i.MX6UL data sheet (1)
USB_OTG2_VBUS	P	X1-42	

3.2.7.6 Power-Up sequence TQMa6ULx / carrier board

The TQMa6ULx meets the required sequencing of the i.MX6UL (7) by using the PMIC (10).
The TQMa6ULx operates with 5 V; the 3.3 V I/O voltage of the i.MX6UL signals is generated on the TQMa6ULx.
This leads to requirements for the carrier board design concerning the chronological characteristics of the voltages generated on the carrier board.

Attention: Malfunction or destruction, Power-Up sequence	
	No TQMa6ULx I/O pins may be driven by external components during the boot-process to avoid cross-supply and errors in the power-up sequence. To ensure a correct power-up, the following sequence must be met on the carrier board: The supply voltage of 5 V for the TQMa6ULx is present and the carrier board supply of 3.3 V is activated by the TQMa6ULx-pin VCC3V3_REF_OUT (X1-17).

The following block diagram shows the control of the voltage regulator on the carrier board:

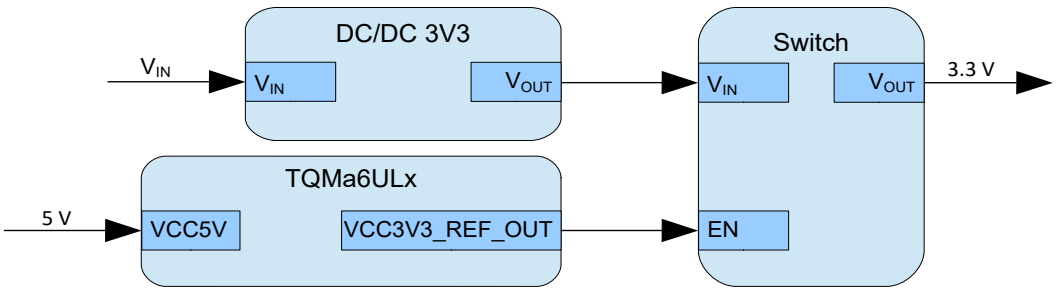


Figure 16: Block diagram power supply carrier board

Note: BOOT_MODE and BOOT_CFG pins supply	
	The BOOT_MODE and BOOT_CFG pins have dedicated reference voltages, which are generated in accordance with the i.MX6UL timing specifications. See also MBa6ULx schematics.

3.2.7.7 Power modes

- Suspend to RAM (deep sleep mode - DSM)
- Standby

DSM and Standby are extremely efficient energy saving modes, in which parts of the core supply are switched off.
Details are to be taken from the i.MX6UL Reference Manual (7). These features have to be supported by the software.

3.2.7.8 PMIC

The characteristics and functions of all pins and signals have to be taken from the i.MX6UL Reference Manual (7) and the PMIC Data Sheet (10). The PMIC is connected to the I2C4 bus of the i.MX6UL.
The following block diagram shows the connection between PMIC and i.MX6UL:

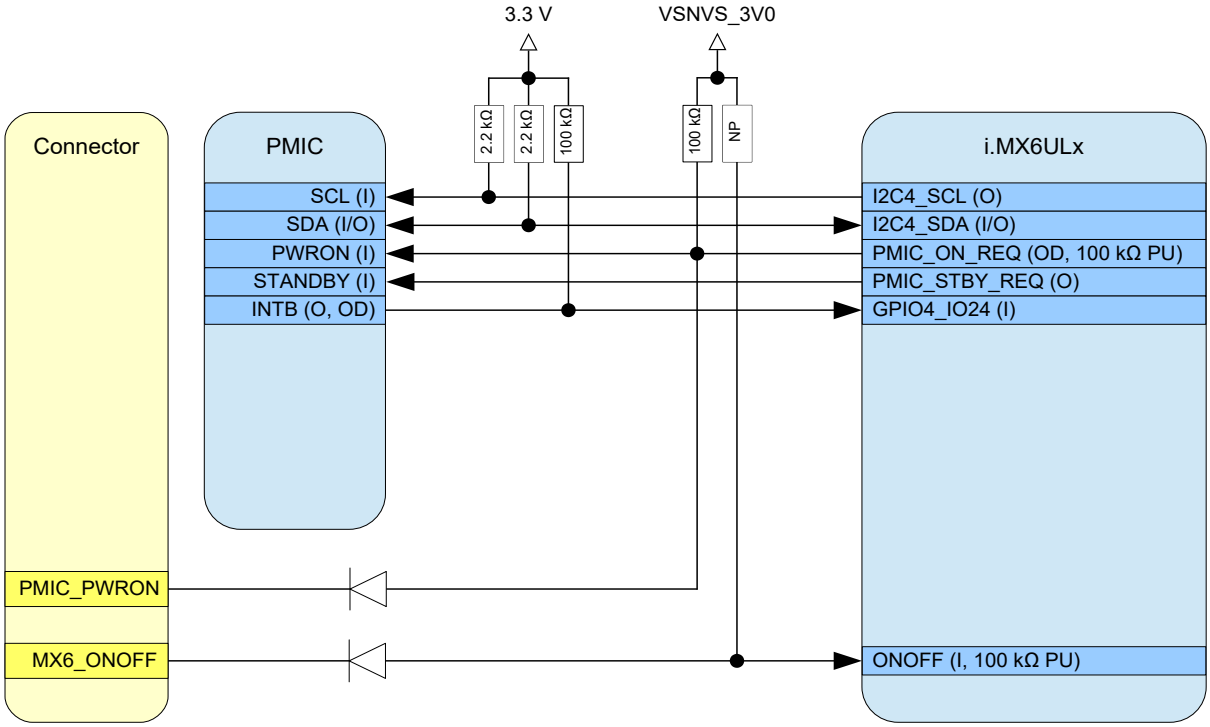


Figure 17: Block diagram PMIC interface

➢ The PMIC has I²C address `0x08 / 000 1000b`

Note: PMIC signal INTB	
	From TQMa6ULx revision 02xx, the PMIC signal INTB can be used via GPIO4_IO24 (X2-91), see Table 22.

Attention: Malfunction or destruction, PMIC programming	
	Improper PMIC programming may cause the i.MX6UL or other peripherals on the TQMa6ULx to operate outside their specification. This can lead to malfunction, deterioration or destruction of the TQMa6ULx.

4. MECHANICS

4.1 Connectors

The TQMa6ULx is connected to the carrier board with two 100-pin connectors.
The following table shows details of the connectors used:

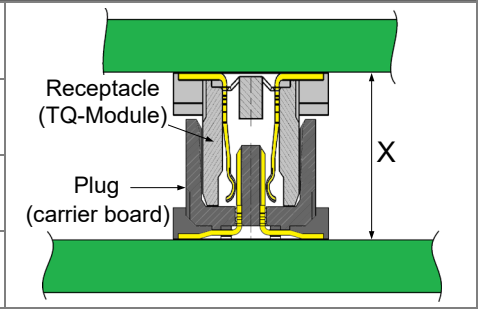
Table 39: Connectors on the TQMa6ULx

Manufacturer	Part number	Remark
TE connectivity	5177985-4	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C … +125 °C

The TQMa6ULx is held in the connectors with a retention force of approximately 20 N.
In order to avoid damage to the TQMa6ULx itself or the connectors on the carrier board caused by mechanical stress during removal of the TQMa6ULx, the use of the extraction tool MOZIA6UL is strongly recommended.

The following table shows suitable mating connectors for the carrier board.

Table 40: Suitable carrier board mating connectors

Manufacturer	Part number	Remark	Stack height (X)	
TE connectivity	5177986-4	On MBa6ULx	5 mm	
	1-5177986-4	–	6 mm	
	2-5177986-4	–	7 mm	
	3-5177986-4	–	8 mm	

The pinout in Table 2 and Table 3 refers to the BSP provided by TQ-Systems.
For information regarding I/O pins in Table 2 and Table 3 refer to the i.MX6UL Data Sheet (1).

4.2 Dimensions

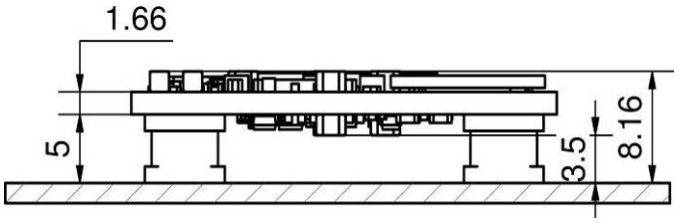


Figure 18: TQMa6ULx dimensions, side view

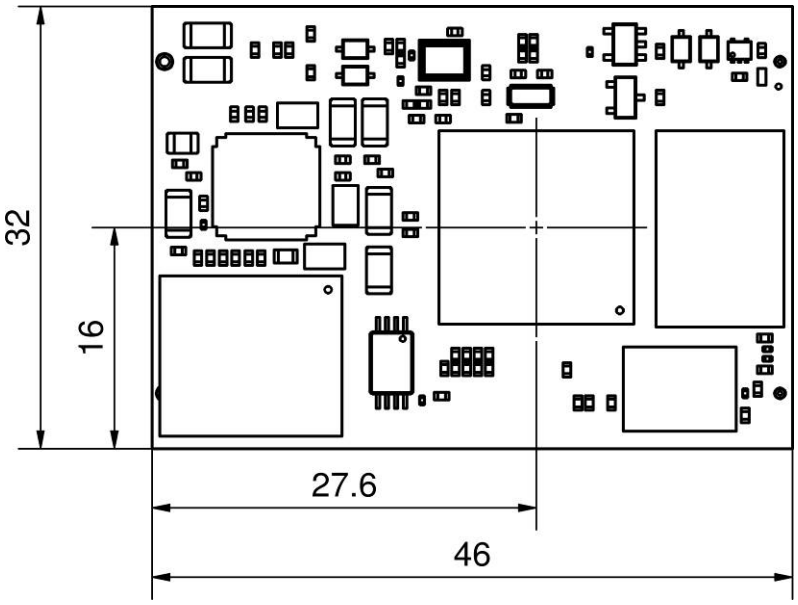


Figure 19: TQMa6ULx dimensions, top view

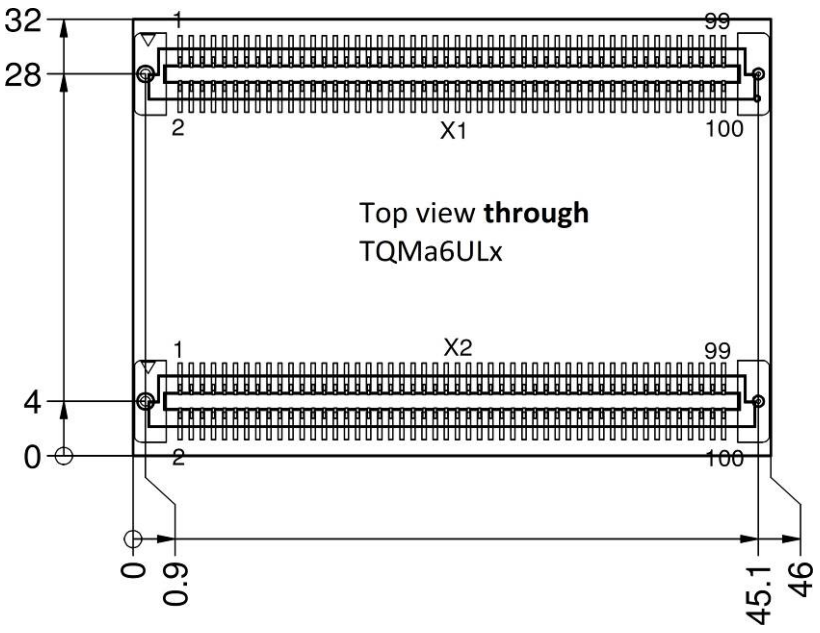


Figure 20: TQMa6ULx dimensions, top view through TQMa6ULx

4.3 Component placement

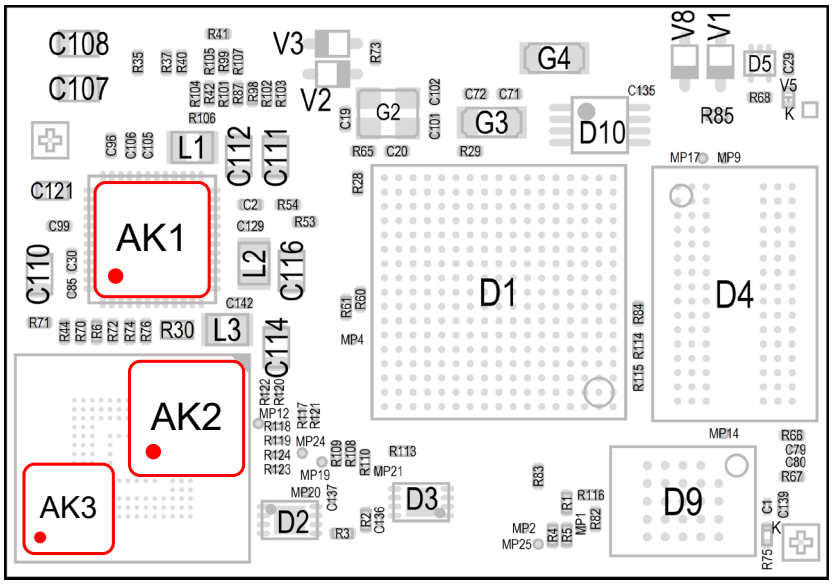


Figure 21: TQMa6ULx component placement top

The labels on the TQMa6ULx show the following information:

Table 41: Labels on TQMa6ULx

Label	Text
AK1	MAC address (+ additional reserved MAC addresses), tests performed
AK2	TQMa6ULx version and revision
AK3	Serial number

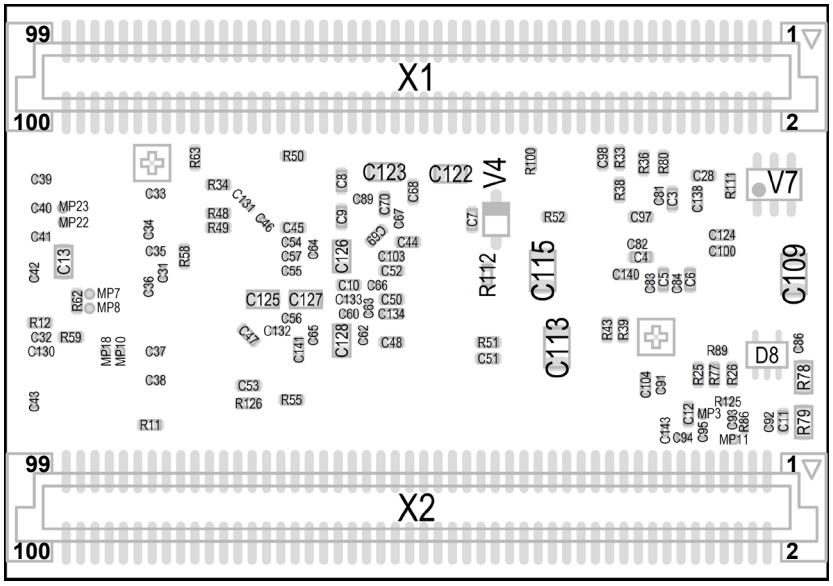


Figure 22: TQMa6ULx component placement bottom

4.4 Adaptation to the environment

The TQMa6ULx has overall dimensions (length × width × height) of 46 × 32 mm × 7.2 mm^3.
The TQMa6ULx has a maximum height above the carrier board of approximately 8.5 mm.
The TQMa6ULx weighs approximately 10 grams.

4.5 Protection against external effects

As an embedded module, the TQMa6ULx is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.6 Thermal management

To cool the TQMa6ULx, on average less than 1 Watt must be dissipated, see Table 36 for peak currents.
The power dissipation originates primarily in the i.MX6UL, the DDR3L SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See NXP documents (3), (4) and (10) for further information.

Attention: Malfunction or destruction, TQMa6ULx cooling	
	The i.MX6UL belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX6UL must be taken into consideration when connecting the heat sink, see (3). The i.MX6UL is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa6ULx and thus malfunction, deterioration or destruction.

4.7 Structural requirements

The TQMa6ULx is held in the mating connectors by the retention force of the pins (200). For high requirements with respect to vibration and shock firmness, an additional retainer has to be provided in the final product to hold the TQMa6ULx in its position. This can be achieved with the combination of heat sink and mounting method. Since no heavy and large components are used, there are no further requirements.

4.8 Notes of treatment

In order to avoid damage to the TQMa6ULx itself or the connectors on the carrier board caused by mechanical stress during removal of the TQMa6ULx, the use of the extraction tool MOZIA6UL is strongly recommended.
The extraction tool MOZIA6UL can also be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa6ULx for the extraction tool MOZIA6UL.

5. SOFTWARE

The TQMa6ULx is shipped with a preinstalled boot loader U-Boot. TQ-Systems GmbH also provides a BSP, which is tailored for the MBa6ULx. The boot loader U-Boot provides TQMa6ULx-specific as well as board-specific settings, e.g.:

- i.MX6UL configuration
- PMIC configuration
- SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

These settings have to be adapted, in case another bootloader is used.
More information can be found in the Support Wiki for the TQMa6ULx.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa6ULx was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

Since the TQMa6ULx operates on an application-specific carrier board, EMC or ESD tests only make sense for the whole device.
The TQMa6ULx it designed to pass the following test:

- EMC-Interference radiation:
  Measurement of the electrically radiated emission for standard, residential, commercial and light industrial environments in the range of 30 MHz to 6 GHz according to DIN EN 55022 A1:2007.

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa6ULx.
Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.4 Climate and operational conditions

The temperature range, for which the TQMa6ULx is designed, strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa6ULx.

Detailed information concerning the thermal characteristics of the i.MX6UL is to be taken from the NXP documents (1) and (6).

In general, a reliable operation is given when following conditions are met:

Table 42: Climate and operational conditions –25 °C … +85 °C

Parameter	Range	Remark
Chip temperature i.MX6UL	–40 °C … +105 °C	Typical max +90 °C
Ambient temperature i.MX6UL	–40 °C … +85 °C	–
Chip temperature PMIC	–40 °C … +125 °C	–
Ambient temperature PMIC	–40 °C … +85 °C	–
Case temperature DDR3L SDRAM	–40 °C … +95 °C	–
Case temperature other ICs	–25 °C … +85 °C	–
Storage temperature TQMa6ULx	–40 °C … +85 °C	–
Relative humidity (operating / storage)	10 % … 90 %	Not condensing

Table 43: Climate and operational conditions –40 °C … +85 °C

Parameter	Range	Remark
Chip temperature i.MX6UL	–40 °C … +105 °C	Typical max +90 °C
Ambient temperature i.MX6UL	–40 °C … +85 °C	–
Chip temperature PMIC	–40 °C … +125 °C	–
Ambient temperature PMIC	–40 °C … +85 °C	–
Case temperature DDR3L SDRAM	–40 °C … +95 °C	–
Case temperature other ICs	–40 °C … +85 °C	–
Storage temperature TQMa6ULx	–40 °C … +85 °C	–
Relative humidity (operating / storage)	10 % … 90 %	Not condensing

6.5 Shock and Vibration

Table 44: Shock resistance

Parameter	Details
Shock	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Residence time	10 msec
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

Table 45: Vibration resistance

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 – 9 Hz, 9 – 200 Hz, 200 – 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X – Y – Z axis
Amplitude	2 Hz … 9 Hz: 3.5 ms^{-2} 9 Hz … 200 Hz: 10 ms^{-2} 200 Hz … 500 Hz: 15 ms^{-2}

6.6 Reliability and service life

The calculated MTBF of the TQMa6ULx is 1,472,325 h at +40 °C ambient temperature, Ground, Benign.

The TQMa6ULx is designed to be insensitive to shock and vibration.

High quality industrial grade connectors are assembled on the TQMa6ULx.

Detailed information concerning the service life of the i.MX6UL under different operational conditions is to be taken from the NXP Application Note (5).

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa6ULx is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa6ULx was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The guideline 2005/32/EC (EuP) is the next step after WEEE® and RoHS for an environmentally friendly production of electric and electronic products. The guideline only applies for products with an annual production quantity of >200,000. The consideration of environmental requirements with the product design "creation appropriate for the environment" ("ecological design") with the aim to improve the environmental compatibility of the product during its whole life cycle should be taken into consideration. The guideline appropriate for the product (embedded PC) is applied.

7.5 Battery

No batteries are assembled on the TQMa6ULx.

7.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa6ULx, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa6ULx is minimised by suitable measures. The TQMa6ULx is delivered in reusable packaging.

7.7 Other entries

The energy consumption of the TQMa6ULx is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 46: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
ASCII	American Standard Code for Information Interchange
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CCM	Clock Control Module
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CSI	CMOS Sensor Interface
DC	Direct Current
DDR3L	Double Data Rate 3 Low voltage
DIN	Deutsche Industrie Norm (German industry standard)
DSM	Deep Sleep Mode
ECSPI	Enhanced Configurable SPI
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIM	External Interface Module
eLCDIF	Enhanced LCD Interface
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
EN	European Standard (Europäische Norm)
ENET	Ethernet
EPIT	Enhanced Periodic Interrupt Timer
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
GPT	General Purpose Timer
HRCW	Hard Reset Configuration Word
I/O	Input/Output
I²C	Inter-Integrated Circuit
I²S	Integrated Interchip Sound
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
IPU	Input with Pull-Up
JTAG®	Joint Test Action Group
KPP	Key Pad Port
LCD	Liquid Crystal Display
LCDIF	LCD Interface
LED	Light Emitting Diode
LICELL	Lithium Cell
LVDS	Low Voltage Differential Signal
MAC	Media Access Control
MII	Media Independent Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MMDC	Multi-Mode DDR Controller
MOZI	Modulzieher (module extractor)
MQS	Medium Quality Sound
MTBF	Mean (operating) Time Between Failures

8.1 Acronyms and definitions (continued)

Table 46: Acronyms (continued)

Acronym	Meaning
n/a	Not Applicable
NAND	Not-And
NC	Not Connected
NOR	Not-Or
NP	Not Placed
OTG	On-The-Go
PC	Personal Computer
PCB	Printed Circuit Board
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down (resistor)
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PU	Pull-Up (resistor)
PWM	Pulse-Width Modulation
PWP	Permanent Write-Protected
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGB	Red Green Blue
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RS-232	Recommended Standard (serial interface)
RTC	Real-Time Clock
RWP	Reversible Write-Protected
SAI	Serial Audio Interface
SD/eSD/SDXC	Secure Digital / enhanced Secure Digital / SD eXtended Capacity
SD/MMC	Secure Digital Multimedia Card
SDIO	Secure Digital Input/Output
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SJC	System JTAG Controller
SNVS	Secure Non-Volatile Storage
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SRC	System Reset Controller
STR	Single Transfer Rate
SVHC	Substances of Very High Concern
SW	Software
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
USDHC	Ultra-Secured Digital Host Controller
VSNVS	Voltage (for) Secure Non-Volatile Storage
WDOG	Watchdog
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 47: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX6UltraLite Applications Processors for Industrial Products IMX6ULxIEC	Rev. 1, 04/2016	NXP
(2)	Chip Errata for the i.MX6UltraLite IMX6ULxCE	Rev. 1, 04/2016	NXP
(3)	AN4871, Application Note Assembly Handling for Lidless FCBGA Packages	Rev. 0, 02/2014	NXP
(4)	AN5170, i.MX6UltraLite Power Consumption Measurement	Rev. 2, 05/2016	NXP
(5)	AN5198, i.MX6UltraLite Product Usage Lifetime Estimates	Rev. 1, 04/2016	NXP
(6)	Hardware Development Guide for the i.MX6UltraLite Applications Processor IMX6ULxHDG	Rev. 1, 03/2016	NXP
(7)	i.MX6UltraLite Applications Processor Reference Manual IMX6ULxRM	Rev. 1, 04/2016	NXP
(8)	i.MX6ULL Data Sheet	Rev. 1.2, 11/2017	NXP
(9)	i.MX6ULL Reference Manual	Rev. 1, 11/2017	NXP
(10)	PF3000, PMIC	Rev. 9, 08/2017	NXP
(11)	MBa6ULx User's Manual	– current –	TQ-Systems
(12)	TQMa6ULx Support-Wiki	– current –	TQ-Systems

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